sondrel

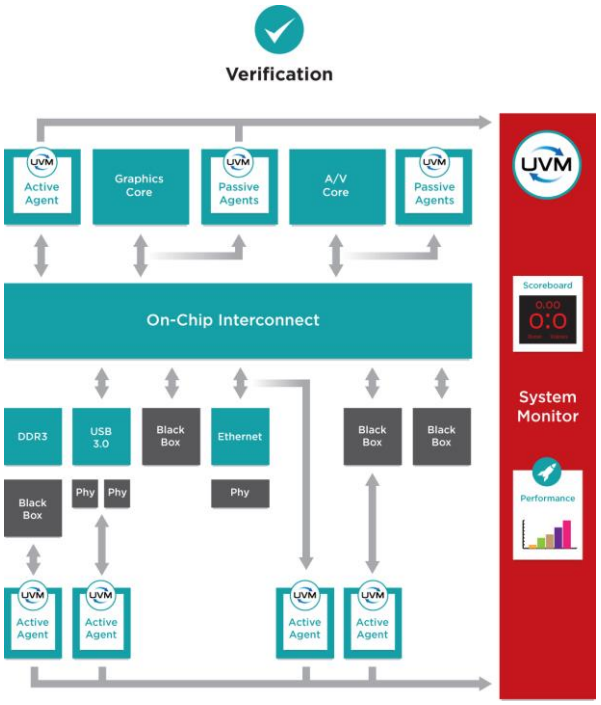
Success through partnership

Functional Verification Consultancy

Functional Verification Consulting Services

Functional verification is often the most resource intensive and costly part of the SoC hardware design process. Sondrel's verification engineering team can enable your verification environment to "shift left", starting verification early in the design cycle by streamlining testbench development, facilitating faster turnaround times and high quality, reliable designs.

Sondrel's expertise covers a comprehensive range of skills including test plan creation, testbench development and design debug at both IP block and SoC level. We are able to bring the latest testbench verification methodologies such as UVM VIP development, ABV and metric driven verification



UVM Testbench

Benefits to customer

Sondrel's functional verification consultancy services can increase the efficiency and effectiveness of your SoC verification.

- Achieve a "shift left" in SoC verification by streamlining testbench development, starting verification earlier
- Access the latest verification methodologies e.g. UVM, ABV, metric driven verification
- Increase verification capacity or leverage low cost design centers
- Achieve higher quality designs with less effort or cost

Engagement Models

Sondrel provides highly flexible engagement models enabling our clients to choose the optimum way of working for their business. Services are delivered through on-site consultants or at our low cost off-shore design centers.

- Metric driven verification, planning, tracking & reporting
- VIP development, porting & configuration
- Testcase development - system or unit level
- Simulation and debug
- Standards: eRM, VMM, UVM, IP-XACT, UCIS, AMBA, MIPI, DDR, USB…
- Languages: Verilog, VHDL, SystemVerilog, e, SVA, PSL, Tcl, Perl, Python, C/C++
- EDA tools: Mentor-Questa, Cadence-Incisive & vManager, Synopsys-VCS, Verdi and Certitude

Technical Details

Functional verification of today's complex SoCs is one of the toughest challenges for the semiconductor industry. It is both resource intensive, requiring a wide range of specialist skills and time consuming. Sondrel's engineers have a wide range of verification skills including simulation based techniques that can be applied at IP block level, sub-system or full chip level. Sondrel can support your existing approach or enhance your capabilities by providing rapid access to the latest technologies such as SystemVerilog, assertion based verification (ABV), UVM and metric driven verification. Each of these technologies increase productivity during verification projects.

SystemVerilog has built-in capabilities designed to support advanced functional verification such as constrained random stimuli, assertions, and coverage points. UVM provides standard libraries designed to make it easier to leverage the capabilities of SystemVerilog and create re-usable verification IP (VIP) components supporting rapid testbench development. The latest simulation tools are optimized for executing UVM testbenches enabling faster testcase throughput.

Adoption of ABV allows design intent to be captured at source so that when errors are detected by assertions, the source of the error is easily traced. Assertions greatly aid observability and reduce time to debug designs.

Sondrel uses the latest verification methodologies to help our clients "shift left" in verification, starting earlier and decreasing time to debug.

Process & Methodology

Sondrel functional verification services support simulation based verification at all stages of the SoC design process from unit level testing to top-level verification of SoCs. We have extensive skills in planning, testbench development, debugging and porting of legacy verification environments to UVM.

Test plans are developed in consultation with the client, including alignment on key metrics, which are tracked using the latest EDA tools.

Testbenches and test stimuli are constructed to deliver the verification plan using re-usable VIP components, constrained random stimuli or if needed directed tests. Where required, legacy VIP can be ported to UVM to improve re-usability and simulation throughput or assertions created to aid debug. Top-level system tests can be created in SW to verify correct function and performance of specific use cases. Tests may be automated to create regression tests or to aid iterative debugging.

Results of simulations are analyzed and reported. Testcases are refined to achieve coverage goals and our verification engineers collaborate with the designers to resolve any bugs that are encountered, throughout the process.

Next Steps

Call us today on
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