# **SFA 350A** Automotive ADAS Chip

# Architecting the future<sup>™</sup>

## AUTONOMOUS VEHICLE QUAD CHANNEL PROCESSOR

### **Features**

ADAS – Advanced Driver Assistance Systems or ADAS are used to support driverless or automatic vehicle applications:

- ASIL B Unit is not directly part of the automatic drive system, system defaults to driver in case of unit failure. (Multiple redundancy would be required for higher ASIL grade).
- ✓ System based on four active sensors, or four passive optical sensors.
- ✓ Active systems use LASER or RADAR illumination of the field of view requiring drive/scanning control and synchronisation with the sensor.

Electronic module compliant to automotive standards, self-contained, vehicle powered, -40°C to 105°C temperature range.

### Take control

Sondrel's reference designs are architected to accommodate bespoke technology requirements, so your chip meets your technical and business needs.

- Differentiate
- Optimise for your parameters
- Protect your IP
- Define security

- Reduce bill-of-material
- Reduce board footprint
- Own your supply chain
- Control time-to-market

# A compelling approach

Sondrel's Architecting the future<sup>TM</sup> designs compress the design lifecycle, reducing time to market compared with designing from scratch. With Sondrel as your ASIC partner, you can rely on our experience to manage the risk and deliver successfully on time, on budget.

SFA 350A is an ADAS -**Advanced Driver Assistance** Systems. ADAS are used to support driverless or automatic vehicle applications.

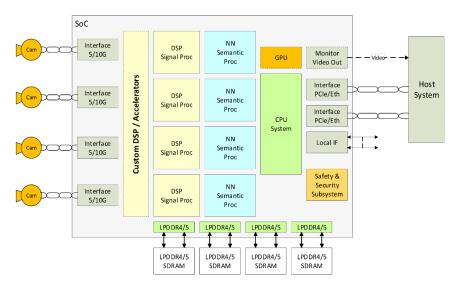
Unit is ASIL B compliant, SoC is ASIL B compliant with an ASIL C/D compliant subsystem for functional safety management.

Communication to the vehicle central unit is via dual redundant link based on standard protocol (for example -Ethernet of PCIe).

Unit has Dual Redundant power supply and clock generation. Compliance with Automotive Grade 2 standard.

## ASIC-based SoC solution:

- Supports custom logic.
- High performance scalable processing options:
  - 0 Compute CPU
  - Signal DSP
  - CNN/RNN NPU 0
- Camera Input, up to:
  - 4K, 30 fps/Cam
  - MIPI IF/others
- **System Communications:** 
  - PCle4 (max x8 lane)
  - Ethernet 1G-10G  $\circ$
- SoC Memory:
  - Scalable Internal RAM
  - LPDDR4+ (x4 lane 64GB/s) or LPDDR5 (x8 lane 128GB/s)
- Safety (FuSa) and Secure (Crypto, Anti-Intrusion) Subsystem
- System Management/Communications Subsystem (extensible/scalable functionality
- <30W, Automotive Grade 2

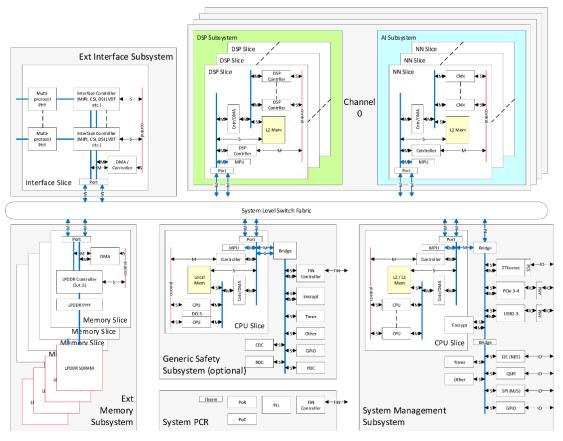






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- Compute Slice Encapsulates multiple cores with standard services.
- Multiple Slices are aggregated for performance in a subsystem.
- Multiple subsystems per Channel (heterogeneous architecture). SoC can support mixed core Slices for tightly coupled heterogeneous compute including custom logic cores/slices.
- Quad Channel SoC

#### Compute Channel

- CPU 1-4 Cores per Slice (1-2GHz)
  - Nom ARM® Cortex® A53/73
  - 9.2-19.2 DMIPS/MHz
- DSP 4 Cores per Slice (1GHz)
  - Cadence® Vision Q7
  - Synopsys<sup>®</sup> EV7x
- NPU 1-2 Cores per slice (1GHz) 10-40 TOP
  - o ARM® Ethos™ Series
  - Synopsys® EV7x-DNN
  - Custom AI

# Time to packaged samples

This chart gives an indication of design duration and time to sample packaged silicon. There is some variability based on your design choices, foundry choice and process node selected. We have full worked pricing for NRE and part costs available – contact us for more details.

