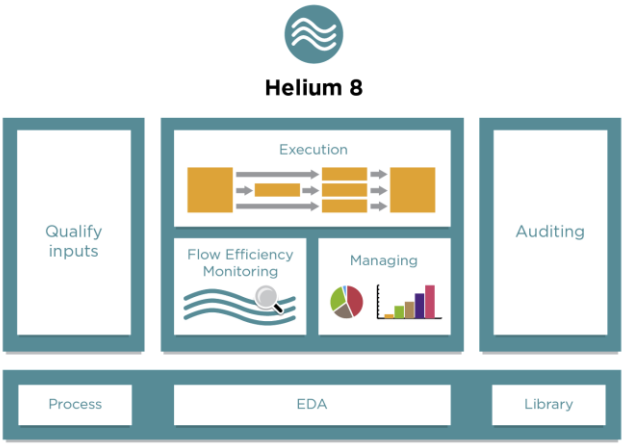
sondrel

Success through partnership

Helium 8 Tool

Optimize Project Execution with Helium 8

A key element in both the technical success and final cost of an RTL2GDSII engagement is the quality of the design methodology & flow. Sondrel's Helium build tool has been developed and refined over ten years and across 250 successful tape outs. 75% of our engagements are at 28nm or below, developing designs up to 700sqmm with some of the world's leading companies and foundries.



Benefits to Client

Helium 8, released in 2015, has been created to deliver low power on large area, advanced node chip designs.

- **Tool independent – can utilize best in class EDA option at each stage in the flow**
- **Allows a quick start to projects, enabling engineers to be productive rapidly**
- **Configurable for differing Price Performance Area priorities (PPA)**
- **Manages project risk, specifying and controlling the design tasks**
- **Interactive GUI gives visualization for improved project management efficiency**
- **Helium 8P (low power option) can save up to 20% dynamic power over alternative build flows**
- **10-20% improvement of the QOR and schedule reduction respect to a non-Helium project examples**

Engagement Models

Typically the engagement will be at one of Sondrel's global ODC locations. Sondrel can supply a liaison manager at the client site.

Engineering Benefits

Helium 8 allows automatic prioritization of project priorities such as PPA, schedule, EDA vendors, technology nodes and library vendors.

The team leader can easily configure the project flow for different activities such as core hardening, complex multi-voltage SoC, or large hierarchical projects.

Uses a set of easy naming conventions, project directories system, documentation, training and labs, so that every engineer is able to work on the system.

Helium 8 can be easily shaped to operate seamlessly within the existing client's flow.

Technical Details

Helium 8 deploys toolbox functions and pre-shaped flow examples that are optimized for various EDA flows (Mentor Graphics, Synopsys, Cadence, Ansys), library vendors (ARM, Synopsys, Avago, TSMC, UMC, etc...), and technology nodes (down to 14nm).

- Bespoke flow and conventions, with revision control support
- Advanced toolbox or scripts templates, to boost the original EDA reference flows
- Easy to configure, portable on different technologies, and interoperable with existing client flows
- Detailed checkpoint auditing functions, to enhance the visibility of the project status and the predictability
- Automated incoming checks, to validate the integration of the intellectual properties of the SOC
- Interactive GUI gives visualization for improved project management efficiency

Table of Technical Details and Capabilities of Helium 8

- Voltage Supply reduction (with library re-characterization)
- Switching activity synthesis and physical optimization
- Latch-based design
- A-OCV and P-OCV
- Phy-aware timing ECO
- Multivoltage (voltage/freq scaling, power gating)
- IRdrop/power aware STA
- Back-biasing
- Memory supply (split core/periphery)
- Self-gating (XOR D/Q)
- CCD optimization
- Top-down approach (blocks timing budgeting and over-constraint reduction)
- Feedthrough optimization
- Slew rate improvement

An option to Helium 8, 8P has been designed to support large SoC projects, on advanced technology nodes, with the power reduction as a priority. Helium 8P supports a mix of techniques that have been successfully applied using different EDA tools, technology nodes and library vendors.

Process & Methodology

Helium supports different types of power intent description (UPF, CPF, or any other specific requirement from the customer). A wide variety of checks are executed (from the Multi-Voltage rule checking, down to the power measure, IRdrop, supply or signal EM, IOs SSO analysis)

Trial implementations will be performed on the design deliverables from the customer and measured against the Helium 8P entry criteria. We work closely with the customer through the Project Leader and via the management system to provide feedback from these checks so helping to improve the quality of the RTL and power and timing constraints.

The internal design flow will be refined by Sondrel to enable implementation of the design and the power targets. This includes aspects such as floor-planning, power routing, clock tree implementation, timing closure and physical closure activities, both at the block and top level.

Next Steps

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