DfT for Automotive

Good practice in DfT during SoC design and verification can improve time to market and reduce manufacturing costs. However, for automotive designs DfT is a critical part of complying with the safety and reliability requirements for this demanding market.

Sondrel’s DfT consulting team is fully conversant with rigorous automotive IC design requirements. They work to optimize the test strategy, complying with the functional safety standard ISO 26262 using ASIL levels (Automotive Safety Integrity Level) specific coverage targets. Sondrel delivers silicon test solutions with optimal test time for the highest coverage.

Benefits to Client

Efficient test strategies with high fault coverage can significantly benefit our clients with higher quality designs and increased product margins.

- Consultancy to guide your design team to develop testable designs
- Reduced physical design costs through good DfT practice
- Optimized test strategies to improve product quality and reduce production test costs
- Ensure packaged silicon delivers required product performance

Engagement Models

Sondrel is happy to provide this specific engineering skill on customer sites working alongside your own design and implementation teams or off-site as an outsourced project through one of our design centers.

- Logic BIST and Hybrid Scan
- At Speed Clocking for Transition, Path-delay and Timing Aware ATPG
- MBIST
- PLLBIST
- Memory Repair
- DfT Verification
- Analogue and Mixed Signal DfT
- Multiple Power Domain Testing
- Test Compression
Technical Details

As more and more functions are integrated on automotive ICs it is becoming increasingly challenging to adequately test these devices in production and ensure self-test during their life cycle. Traditional scan techniques alone are just too slow and do not take into account automotive safety requirements. They lack capacity and do not offer the capability of self-test of the device during the real application. As a result, new DfT techniques have been introduced to address the challenges. These techniques increase the testability of the design and reduce production test times, but require additional design effort across multiple disciplines. Sondrel is able to support your design teams in accessing these techniques, in addition to more standard DfT techniques whilst delivering optimal production test strategies in your products.

To meet the quality and reliability requirements of the ISO 26262 and other automotive electronics standards “infield” chip testing is necessary. Logicbist provides an infield and system testing method throughout the product life cycle and can also be used for fast manufacturing test bring up, thereby reducing expensive test time.

Internal JTAG P1687 is also supported by Sondrel. UTAG replaces ad-hoc communication methods for controlling on-chip test structures and embedded instruments enabling higher degrees of interoperability and DfT re-use. This allows easier integration of on-chip embedded instruments such as PLL, BIST and memory BIST with sophisticated memory test pattern generation and repair.

Sondrel also has experience with high-end ATPG supporting several fault models including stuck-at and path delay and simulate and verify that the test patterns will execute as part of the design process. We also can provide help with post-silicon debug through shmoo plot analysis and tester log assisted simulation.

Process & Methodology

DfT tasks are included in Sondrel’s award winning Helium flow. The design methodology used by Sondrel is test-driven, with testability considerations influencing every major step of the design process.

Today’s EDA tools enable a large degree of automation in the DfT flow. However it is still necessary that DfT guidelines are applied during RTL design to ensure that the design is highly testable. Optimal implementation of the Sondrel DfT guidelines will ensure the best test QoR (highest coverage/lowest test time).

DfT for complex SoC designs cannot be considered in isolation. Physical design has a significant impact on the DfT implementation. Sondrel’s expertise in physical design pays dividends for DfT ensuring:

- Optimal partitioning of test compression.
- Architecture of memory BIST controllers
- STA of test modes to ensure that DfT minimises impact on functional timing closure.

Once the test features have been implemented Sondrel will generate and verify the test patterns and will help with the transfer of the patterns to the test house of your choice.

If any issues are identified during post-silicon validation, Sondrel is experienced in working with diagnostic tools in order to identify design issues and to enhance the test vectors to accommodate any changes that may be required.

Next Steps

Call us today on 0118 983 8550 or email info@sondrel.com