# Design for Test (DfT) Consultancy

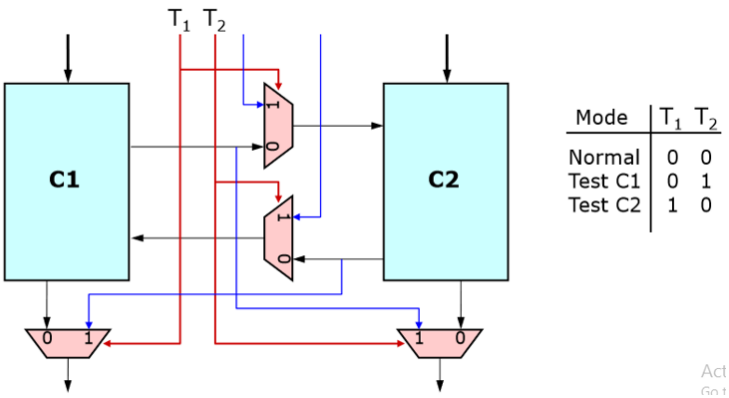
Success through partnership

## DfT Consulting Services

Good practice in DfT during SoC design and verification can improve time to market and reduce manufacturing costs.

Sondrel's DfT consulting services deliver testable silicon with optimal test time. As part of an outsourced project engagement, or as an embedded member of our client's design team, Sondrel can provide specialist DfT consulting expertise.

Our engineers will work to optimize the test strategy meeting the target test coverage requested by the customer in the most efficient way.




| Mode | $T_1$ | $T_2$ |
|---|---|---|
| Normal | 0 | 0 |
| Test C1 | 0 | 1 |
| Test C2 | 1 | 0 |

**Core Based Dft Strategy for Complex SoC**

## Benefits to Client

Efficient test strategies with high fault coverage can significantly benefit our clients with higher quality designs and increased product margins.

- Consultancy to guide your design team to develop testable designs
- Reduced physical design costs through good DfT practice
- Optimized test strategies to improve product quality and reduce production test costs
- Ensure packaged silicon delivers required product performance

## Engagement Models

Sondrel is happy to provide this specific engineering skill on customer sites working alongside your own design and implementation teams or off-site through one of our design centers.

- MBIST, PLLBIST, Logic BIST and Standard Scan
- Memory Repair
- DfT Verification
- Analogue and Mixed Signal DfT
- Multiple Power Domain Testing
- Test Compression
- At Speed Clocking for Transition, Path-delay and Timing Aware ATPG

## Technical Details

As more and more functions are integrated into complex SoCs it is becoming increasingly challenging to adequately test these devices in production or test them in a way that does not adversely affect the product cost. Traditional scan techniques are just too slow, lack capacity or do not sufficiently test that the chip will function correctly. As a result new DfT techniques have been introduced to address the problem. These techniques increase the testability of the design and reduce production test times, but require additional design effort across multiple disciplines. Sondrel is able to support your design teams in accessing these techniques, in addition to more standard techniques like boundary scan and scan chains. We are able to implement these techniques to deliver optimal production test strategies in your products.

Core based testing uses multiple scan chains to divide and conquer testing of large SoCs, whilst test compression takes advantage of the significant redundancy in ATPG scan patterns to compress the vectors applied at the chip boundary and reconstruct the patterns on-chip at high speed, increasing tester throughput.

JTAG P1687 can replace ad-hoc communication methods for controlling on-chip test structures and embedded instruments enabling higher degrees of interoperability and DfT re-use. This allows easier integration of on-chip embedded instruments such as PLL BIST and memory BIST with sophisticated memory test pattern generation and repair.

Sondrel also has experience with high-end ATPG supporting several fault models including stuck-at and path delay. We are able to simulate and verify that the test patterns will execute. We also provide help with post-silicon debug through shmoo plot analysis and tester log assisted simulation.

## Process & Methodology

DfT tasks are included in Sondrel's award winning Helium flow. The design methodology used by Sondrel is test-driven, with testability considerations influencing every major step of the design process.

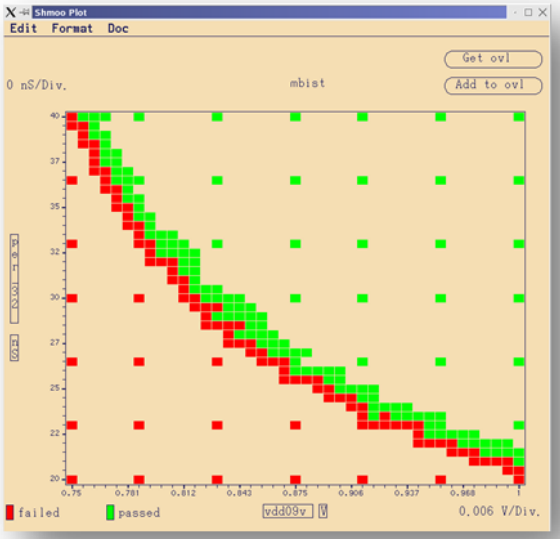
Today's EDA tools enable a large degree of automation in the DfT flow. However it is still necessary that DfT guidelines are applied during RTL design to ensure that the design is highly testable. Optimal implementation of the Sondrel DfT guidelines will ensure the best test QoR (highest coverage/lowest test time).

DfT for complex SoC designs cannot be considered in isolation. Physical design has a significant impact on the DfT implementation. Sondrel expertise in physical design pays dividends for DfT ensuring:

- Optimal partitioning of test compression.
- Architecture of memory BIST controllers
- STA of test modes to ensure that DfT minimises impact on functional timing closure.

Once the test features have been implemented Sondrel will generate and verify the test patterns and will help with the transfer of the patterns to the test house of your choice.

If any issues are identified during post-silicon validation, Sondrel is experienced in working with diagnostic tools in order to identify design issues and to enhance the test vectors to accommodate any changes that may be required.




**Shmoo Plot Analysis**

## Next Steps

Call us today on
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